forming a local interconnection in a range which passes through the first opening and the second opening and contains at least a region where the upper electrode contacts with the oxide dielectric film, by patterning the metal film, wherein the local interconnection is a blocking layer for preventing a diffusion of a redundant to the oxide dielectric film; and

forming a third insulating film for covering the local interconnection.

REMARKS

By this Amendment, claims 1, 5, 11 and 14 have been amended, and new claim 21 has been added. The applicants respectfully submit that no new matter has been added. It is believed that this Response is fully responsive to the Office Action dated April 12, 2000.

Title of the Invention:

The title of the invention has been objected to for being non-descriptive of the applicants' claimed invention. The applicants respectfully request reconsideration of this objection.

As indicated above, the title of the invention has been amended, in its entirety, so as to read as follow:

METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE HAVING CAPACITOR.

It is believed that such amended title of the invention is now descriptive of the claimed invention.

In view of the above, the applicants respectfully request that the title of the invention, as submitted herewith, be approved by the Examiner, and that the outstanding objection to the title be withdrawn.

35 U.S.C. §112, Second Paragraph, Rejection:

Claims 1 - 16 stand rejected under 35 U.S.C §112, second paragraph, due to certain informalities, which the Examiner deemed needed correction, as specifically set forth in item 5, pages 2 and 3 of the outstanding Action.

This rejection is respectfully traversed.

Applicants respectfully submit that the amendments to claims 1, 5, 11 and 14 obviates the rejection of claims 1 - 16 under 35 U.S.C. §112, second paragraph. Accordingly, withdrawal of the rejection of claims 1 - 16 under 35 U.S.C. §112, second paragraph, is respectfully solicited

As to the Merits:

As to the merits of this case, the Examiner sets forth the following rejections:

(1) claims 1 - 16 stand rejected under 35 U.S.C. 102(e) as being anticipated by **Mochizuki et al.** (U.S. Patent No. 5,990,507); and

(2) claims 1 - 13 and 16 stands rejected under 35 U.S.C. 103(a) as being unpatentable over **Ochiai** (U.S. Patent No. 5,943,583) or **Watanabe et al.** (U.S. Patent No. 5,481,490) taken with **Zafar** (U.S. Patent No. 5,750,419) in view of **Kawai et al.** (U.S. Patent No. 6,022,774) and **Yamazaki et al.** (U.S. Patent No. 6,046,469).

All of these rejections are respectfully traversed.

Claim 1 is characterized by comprising the steps of forming an impurity diffusion layer in a semiconductor substrate, forming a first insulating film on the semiconductor substrate, forming a lower electrode, an oxide dielectric film and an upper electrode as a capacitor, forming a second insulating film on the capacitor, forming a first opening on the impurity diffusion layer and a second opening on the upper electrode in the first and second insulating film, forming a metal film on the second insulating film for connecting the diffusion layer and the upper electrode, forming a local interconnection in a range which contain at least a region where the upper electrode contacts with the oxide dielectric film and forming a third insulating film.

In other words, it is a matter defining the invention to form a local interconnection in a range which contain at least a region where the upper electrode contacts the oxide dielectric film.

It is a purpose of the invention to prevent deterioration of polarization characterization caused by a diffusion of hydrogen which is a reduction gas, in the case of forming the third insulating film on the capacitor by a CVD using the reduction reaction.

Therefore, the local interconnection is formed in a range which contain at least a region where the upper electrode contacts with the oxide dielectric film, and the local interconnection become the layer for preventing the diffusion of the hydrogen.

Claim 1 has been rejected from the following five cited documents.

(1) As to rejection from novelty

It has been rejected by a reason that claim1 does not have novelty from Mochizuki (U.S. Patent No. 5,990,507)

It is disclosed in the Mochizuki that a cited invention comprising the steps of forming a impurity diffusion layer in a semiconductor substrate, forming a first insulating film, forming a first opening on the impurity diffusion layer, forming a plug by embedding a refractory metal to the opening on the impurity diffusion by a metal CVD method, forming a lower electrode, an oxide dielectric film and an upper electrode as a capacitor on the first insulating film, forming a second insulating film, forming a second opening on an upper portion of the plug and the upper electrode, forming a local interconnection for connecting the plug on the diffusion layer and the upper electrode and forming a third insulating film.

A purpose of the Mochizuki is to prevent deterioration of polarization-characterization. Hereupon the Mochizuki gives problems that when a interconnection is formed by a metal CVD method or MO-CVD method which have a good step coverage after the oxide dielectric film is formed, a characterization of a capacitor is deteriorated by a diffusion of hydrogen which is a reduction gas.

But it is not described that the problems of a diffusion of hydrogen to an oxide dielectric film in a step of forming an insulating layer on a capacitor by a CVD method as claim 1.

not in claim 1

For solving this problem, the Mochizuki comprises the steps of forming the flattened first insulating, forming the opening on the diffusion layer embedding the refractory metal to the opening and forming a plug. Since an under interlayer is formed flatly, an interconnection can be formed on a capacitor by a sputtering method not using a reduction gas as a hydrogen. In this matter, it can prevent deterioration of a capacitor characterization.

In other words, the interconnection in the Mochizuki is not used as a blocking layer of hydrogen like claim 1 and Mochizuki is the devised invention as not may use process using hydrogen after forming a capacitor.

It is not described in the step of forming an interconnection of the Mochizuki that the interconnection is formed in a range which contain at least a region where the upper electrode contacts with the oxide dielectric film as claim 1.

The interconnection 22 is formed in an outside of the upper electrode in the sectional views Fig. 21 etc of the Mochizuki, but the interconnection layer 22 is formed an inside of the upper

electrode in the plan view (Fig. 8) clearly. In addition, while a TiN film as an interconnection in the Mochizuki is disclosed, it is not described that the TiN film is a blocking layer for preventing a diffusion of hydrogen.

Accordingly the persons skilled in the art can not invent easily that forming an interconnection in a range which contain at least a region where the upper electrode contacts the oxide dielectric film for preventing a diffusion of hydrogen in the step of forming a insulating film on a capacitor.

As the above description, it is different between claim 1 and the Mochizuki in the point that claim 1 comprises the steps of forming an interconnection in a range which contain at least a region where the upper electrode contacts the oxide dielectric film for preventing a diffusion of hydrogen, and claim 1 makes it a matter defining the invention, but the Mochizuki does not make it a matter defining the invention.

Accordingly, since a constitution and a derived advantage are different between claim 1 and the Mochizuki, we allege that claim 1 has novelty.

(2) As to rejection from non-obviousness

It has been rejected from four cited documents by a reason that claim 1 does not have non-obviousness.

Ochiai (U.S. Patent No. 5,943,583)

It is disclosed in the Ochiai that a cited invention comprising the steps of forming a impurity diffusion layer, forming a first insulating film, forming a lower electrode, an oxide dielectric film

and an upper electrode as a capacitor, forming a second insulating layer, forming a opening on the impurity layer, embedding a diffusion preventing film to the opening layer annealing for decreasing a contact resistance, removing the diffusion preventing film, forming, forming a opening on the upper electrode and forming a interconnection for connecting the opening and the upper electrode.

In other words, a purpose of the Ochiai is to prevent a diffusion of a impurity which causes a junction leak of a transistor from an oxide dielectric film consisting of PZT etc in the step of the annealing for descreasing a contact resistance.

It is not described in the step of forming an interconnection of the Ochiai that the interconnection is formed in a range which contain at least a region where the upper electrode contacts with the oxide dielectric film as claim 1. And the interconnection is clearly formed in an outside of the upper electrode in Fig. 4 of the Ochiai.

not true

Accordingly, since a purpose and a constitution of the invention is different between claim 1 and the Ochiai completely, we allege that claim 1 has non-obviousness.

Watanabe (U.S. Patent No. 5,481,490)

A step similar to Ochiai is disclosed in the Watanabe.

The result of the investigation of Watanabe is similar to the one of the Watanabe.

Zafer (U.S. Patent No. 5,750,419)

It is disclosed in the Zafer that a cited invention comprising the steps of forming a impurity diffusion layer in a semiconductor substrate, forming a first insulating film on the semiconductor substrate, forming a lower electrode, an oxide dielectric film and an upper electrode as a capacitor,

forming a second insulating film on the capacitor, forming opening on the impurity diffusion layer the upper electrode, forming a interconnection for connecting the diffusion layer and the upper electrode and forming a third insulating film.

Kawai (U.S. Patent No. 6,220,774)

It is disclosed in the Kawai that a cited invention comprising the steps of forming an impurity diffusion layer and a salicide layer in a semiconductor substrate, forming a first insulating film, forming a lower electrode, an oxide dielectric film and an upper electrode as a capacitor, forming a second insulating film on the capacitor, forming opening on the impurity diffusion layer the upper electrode, forming a interconnection for connecting the diffusion layer and the upper electrode and forming a third insulating film.

A purpose of the Kawai is to prevent an oxidation of the impurity diffusion layer in the step of the annealing with an oxygen for recover a deterioration of the oxide dielectric film after the opening of the impurity diffusion layer is prevented by forming the salicide on the impurity diffusion layer.

It is not described in the step of forming an interconnection of the Kawai that the interconnection is formed in a range which contain at least a region where the upper electrode contacts with the oxide dielectric film as claim 1.

But the interconnection layer is formed in a range which contain at least a region where the upper electrode contacts the oxide dielectric film in Fig. 2H of the Kawai. Since a plan view of the interconnection and the upper electrode is not disclosed and the purpose of claim 1 is described, it

is not suggested that the interconnection is formed in a range which contain at least a region where the upper electrode contacts the oxide dielectric film as claim 1.

Accordingly, since a purpose, a constitution and an advantage are difference between claim 1 and the Kawai, we allege that claim 1 has non-obviousness.

Thus, for at least these reasons, it is respectfully asserted that the prior art fails to teach or suggest recitations of claims 1-16 and 21, and request that the Examiner allow these claims, along with the entire application, to issue. Accordingly, withdrawal of the rejection of claims 1-16 under 35 U.S.C. §102 and §103 is respectfully solicited.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

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